CONTROL DATA CORPORATION

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APPLICATION NOTE

PLO AND WRITE PRECOMPENSATION FOR 5.25 INCH FDD'S

MAGNETIC PERIPHERALS, INC.
a Control Data Company

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APPLICATION NOTE

PLO AND WRITE PRECOMPENSATION WITH CONTROL DATA 5.25 INCH FLEXIBLE DISK DRIVES

INTRODUCTION

This note is intended to inform the flexible disk controller designer about read/write circuitry recommended to achieve maximum data recovery and reliability. The note includes a detailed discussion of common data recovery problems, recommended solutions, circuit specifications, and circuit designs which have been proven with Control Data Flexible Disk Drives.

The note is divided into three sections: (1) Phase-Lock Oscillator Circuits; (2) Problems with synchronous Counter Circuits; and (3) Write Precompensation.

For additional information, contact your local CDC Sales Office or the Applications Engineering Department.

1.1 NEED FOR A PHASE LOCK OSCILLATOR

Refer to the appropriate Flexible Disk Drive Product Specifications:

FDD 9408 Product Specification 77641902 and 77653566
FDD 9409 Product Specification 77653379
FDD 9409T Product Specification 77653489
FDD 9428 Product Specification 77715891
FDD 9429 Product Specification 77715860
FDD 9430 Product Specification 77715892

A. RECORDING METHODS

1. Frequency Modulation (FM)

Data cells are defined by the presence of a flux reversal (clock) at each boundary between adjacent data cells. (Boundary in this context means the leading or trailing edge of a data cell.) A "1" bit is recorded as a flux reversal in the center of a data cell. A "0" bit is recorded as the absence of a flux reversal within a data cell.

FM recording is sometimes called "Single Density" or Double Frequency (DF) recording. The number of flux reversals varies from a maximum of two reversals per bit (all "1"s) to a minimum of one reversal per bit (all "0"s).

FM recording is self clocking and provides synchronization for data separation using simple one shot techniques. However, use of a phase lock oscillator (PLO) instead of a simple one shot system will increase operating margins and result in greater data reliability with more tolerance for media imperfections.

2. Modified Frequency Modulation (MFM)

A "1" bit is recorded as a flux reversal in the center of a data cell. A "0" bit is recorded as the absence of a flux reversal within a data cell. "Clock" flux reversals occur only at the boundary between adjacent cells containing "0's". "Clock" flux reversals are suppressed at both boundaries of every data cell containing a "1" bit.

In MFM recording the number of flux reversals varies from a maximum of one reversal per bit (all "1's" or all "0's") to a minimum of one reversal for every two bits (alternating "1's" and "0's"). Flux reversals never occur closer to each other than the duration of one full data cell. Therefore, the duration of each data cell may be reduced to one half the duration of a data cell in FM recording while maintaining the same minimum interval between flux reversals.

Modified frequency modulation (MFM) recording doubles the data storage capacity. Since the MFM coding technique is not self clocking, it is necessary to generate a synchronized clock from the data stream. If both single and double density systems are being used, the same PLO can serve both applications.

B. DATA RECOVERY

1. Frequency Modulation (FM)

When using frequency modulation recording mode, Control Data recommends the use of a phase lock loop oscillator (PLO) to recover data. The use of a PLO tends to average out peak shift components without the doubling effect associated with the use of a one shot data separator. A PLO has the capability to track long and short term timing variations in the data stream. The use of a PLO will increase operating margins and result in greater data reliability with more tolerance for media imperfections.

2. Modified Frequency Modulation (MFM)

When using the modified frequency modulation (MFM) or double density encoding scheme, a PLO is required because the MFM coding is not self clocking. The PLO is used to generate a synchronized clock from the data stream. The same PLO can be used for single density (FM) and double density (MFM) recording modes. The recommended PLO's have an input to allow the controller to select the recording mode.

1.2 BLOCK DIAGRAM OF A PLO CIRCUIT

Figure 1-1 is a block diagram of a phase lock oscillator and data separator circuit.

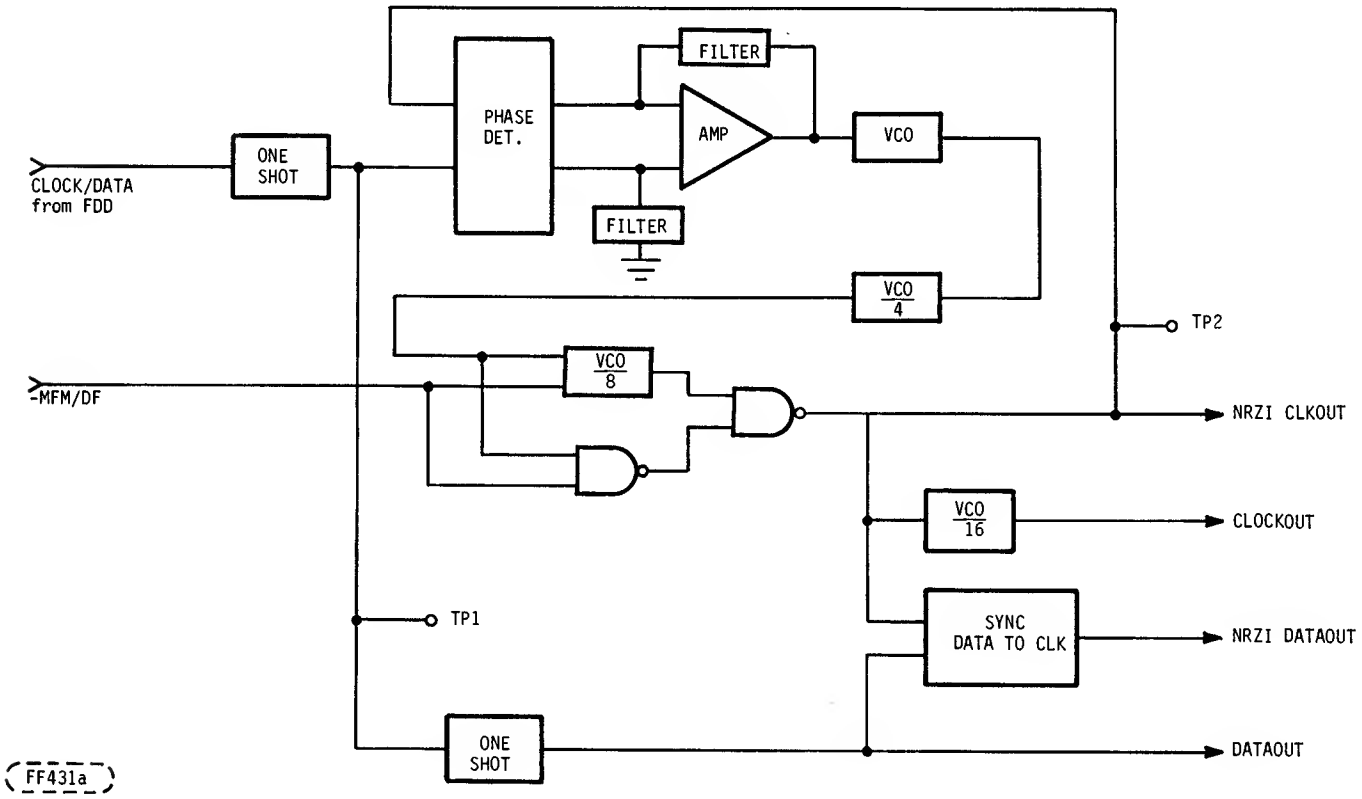


FIGURE 1-1. PLO BLOCK DIAGRAM

1.3 THEORY OF OPERATION

For the most reliable data recovery from flexible disk drives, a clock pulse should be created and synchronized to the Read Clock/Data from the drive. A phase lock loop circuit is used to accomplish this synchronization. The next step for reliable operation is the separation of the clock and data after it has been synchronized to the host system clock. This is accomplished by using a one shot and flip flop combination, synchronized by the clock pulse generated by the PLO.

Phase Locked Oscillator Circuit from Discrete Components

Refer to Figure 1-1.

The heart of the Phase Locked Oscillator (PLO) circuit is a Voltage Controlled Oscillator (VCO) which free runs at 2 MHz. Half of the Motorola MTTL Complex Functions, MC4024 Dual Voltage Controlled Multibrator is used for the VCO. The output is divided by eight for FM operation and divided by four for MFM operation. This basic PLO circuit was designed for use with 8 inch flexible disks with the exception that the output of the VCO has an extra divide by two functions to accommodate the 5.25 inch transfer rate. The best way to get stable operation out of the MC4024 is to use the 2 MHz free running state. Reducing input quiescent value and decreasing oscillator capacity would not result in as stable operation at the required frequencies.

The NRZ clock out signal (125 kHz for FM or 250 kHz for MFM) is compared to the reshaped input read Clock/Data signal from the drive. There are three possible results of this comparison:

1. The Read Clock/Data leads the VCO signal. When this is true a small pulse appears on the minus input to the Op Amp. As the input of the Op Amp goes more negative the output goes more positive thus increasing the VCO frequency. This frequency increase causes the training edges of the NRZ clock pulses to come closer to the trailing edges of the Read/Clock/Data pulses.

2. The VCO signal leads the head Clock/Data. A small pulse appears on the plus input to the Op Amp, causing the output to go more negative reducing the VCO frequency. This frequency decrease causes the trailing edges of the NRZ clock pulses to come closer to the trailing edges of the read Clock/Data pulses.

3. Read Clock/Data and VCO signals coincide. No pulses are transferred to the Op Amp and therefore no frequency adjustment is made to the VCO. However, due to the spindle speed variations and circuit variations, there will be a constant correction process to keep the Read Clock/Data and VCO signals in phase.

The result is a VCO clock output, phase locked to the Read Clock/Data input. The circuit provides the capability to select FM or MFM data recovery with the option of NRZ Clock Out and Clock Out with NRZ Data Out or Data Out. The PLO synchronizes the generated clock with the data, and additional circuitry seapartes clock and data for system processing.

The operating specifications for this circuit are as follows:

Free Running Frequency	2 MHz
Capture Range	±15%
Lock Up Time: 5.25 Inch FDD	100 µs "1111" or "0000" pattern
	200 µs "1010" pattern

5.25 Inch FDD Timing

The PLO circuit operation is basically the same for MFM or FM operation. The data cell time for MFM is four microseconds (eight microseconds for FM), so the Shaped Data pulse is one microsecond wide for MFM and two microseconds wide for FM. For MFM the VCO output is divided by four; for FM it is divided by eight.

The incoming Read Data signal is shaped by the one shot to match the pulse width of the Feedback from the voltage controlled oscillator (VCO) in either MFM or FM mode.

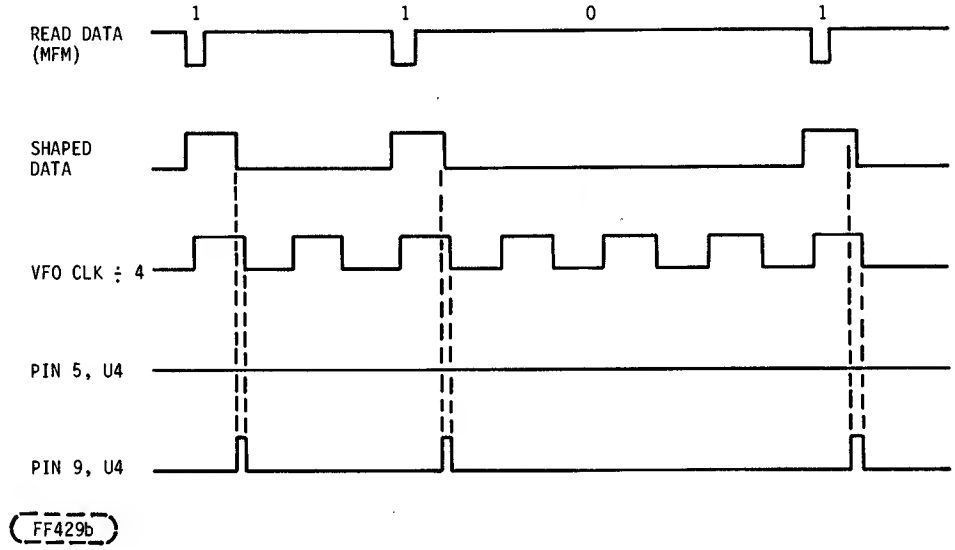


FIGURE 1-2. VFO CLK ÷ 4 LAGGING SHAPED DATA

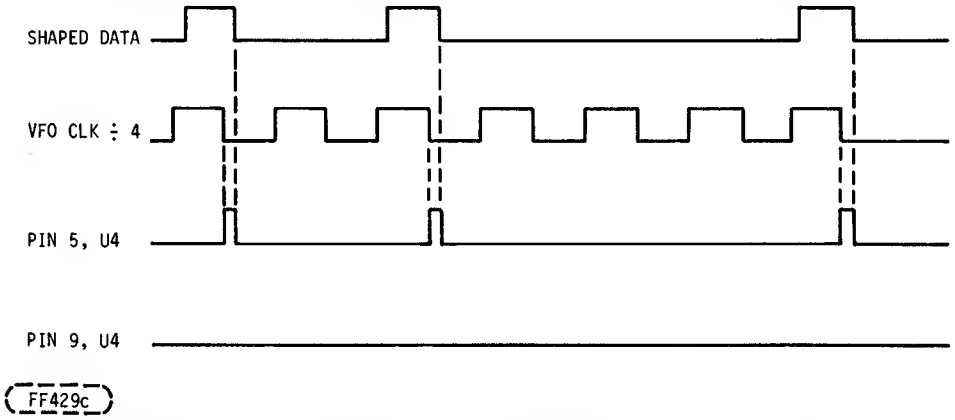


FIGURE 1-3. VFO CLK ÷ 4 LEADING SHAPED DATA

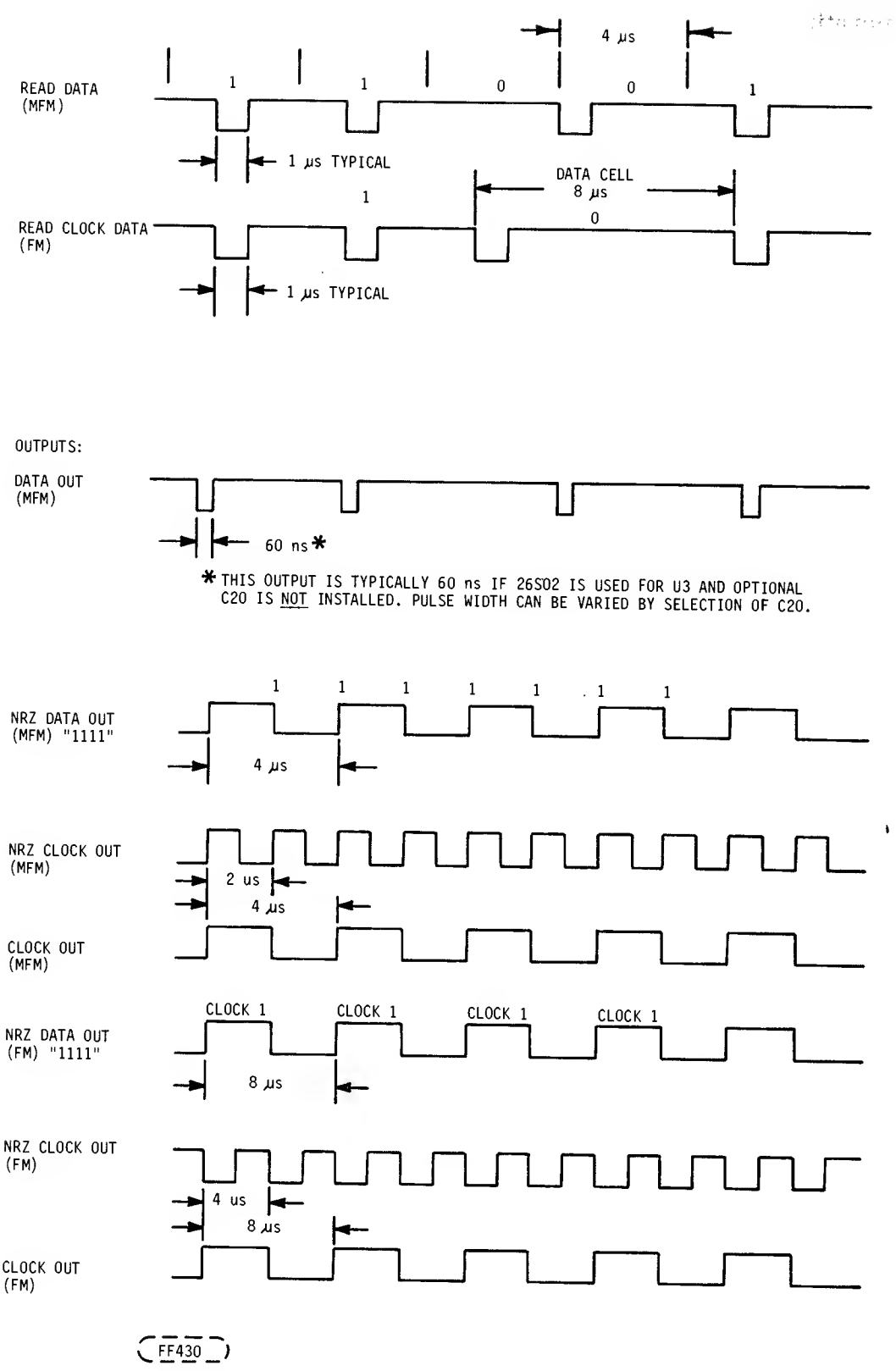


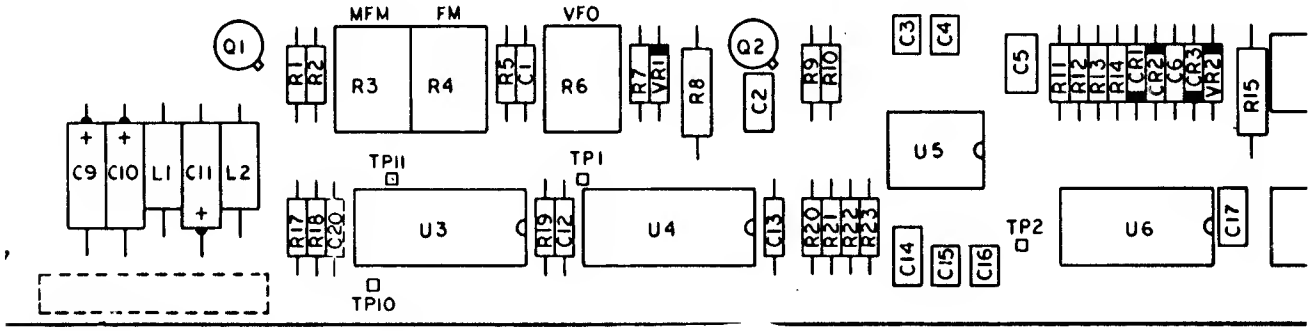
FIGURE 1-4. WORST CASE PATTERNS

1.4 MPI PLO CIRCUIT LAYOUT, VOLTAGE TOLERANCES, COMPONENT TOLERANCES

The PLO circuit contains some analog circuitry that requires close attention to layout, voltage tolerances, and component tolerances. Figure 1-5 shows a recommended layout and ground plane for this portion of the PLO circuit. Also shown are the recommended supply voltage filter components which have the following values:

+5 V	C9 - 33 uF	10 V
-12 V	C10 - 10 uF	15 V
	L1 - 10 mH	
+12 V	C11 - 10 uF	15 V
	L2 - 10 mH	

COMPONENT LAYOUT



GROUND PLANE

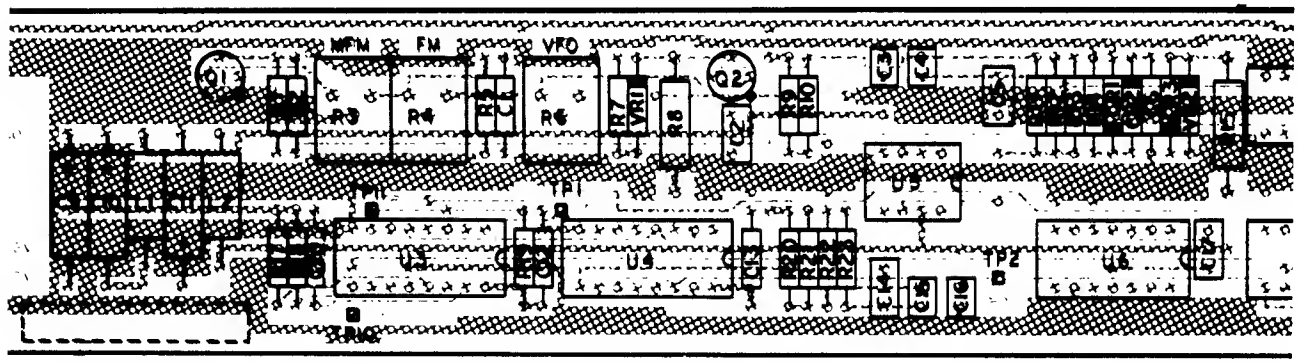


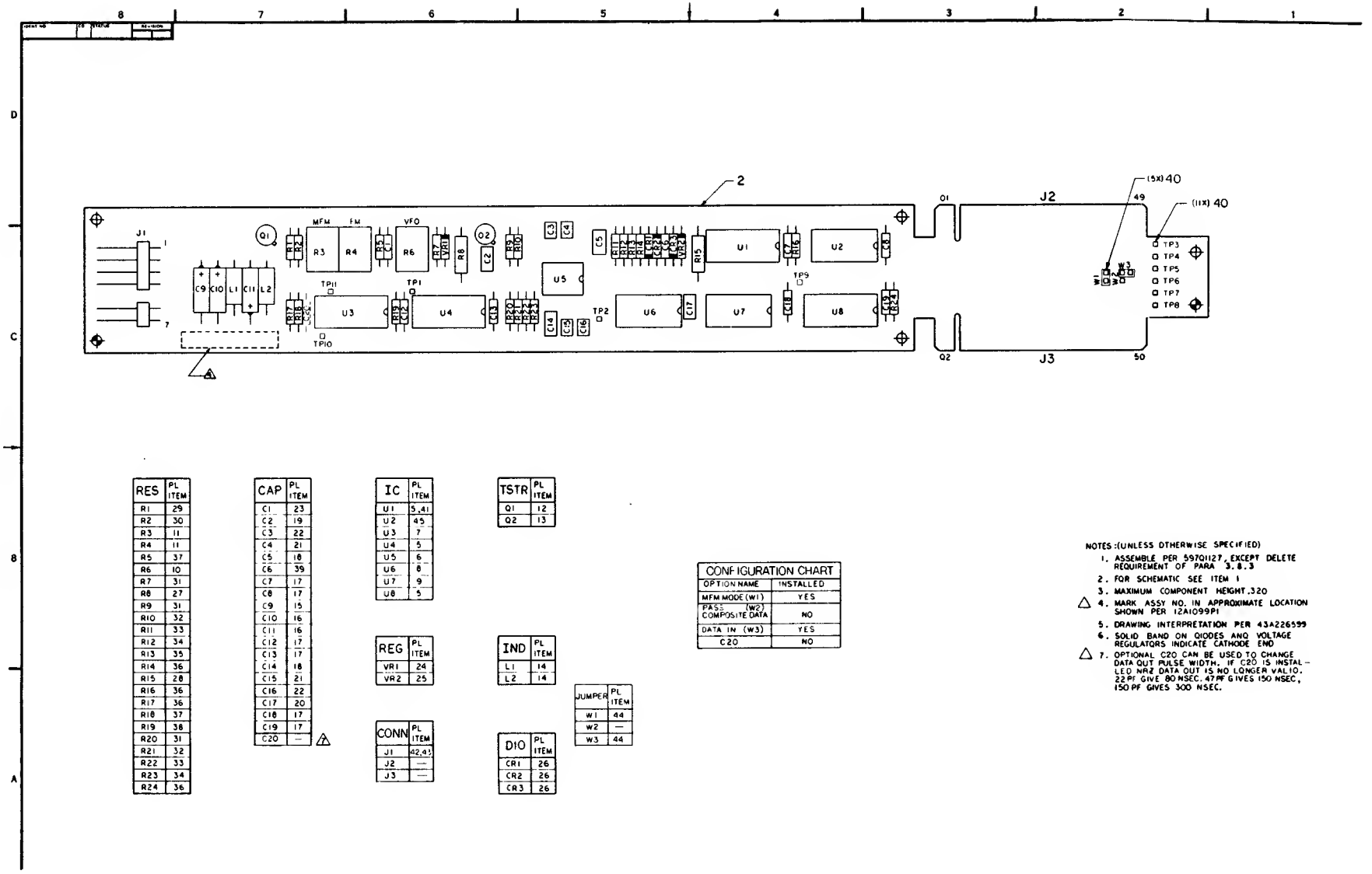
FIGURE 1-5. RECOMMENDED PLO COMPONENT LAYOUT AND GROUND PLANE

The voltage tolerances on this circuit for all voltages is ±5 percent. Component tolerances are as follows unless noted otherwise.

Capacitors	±20%
Resistors	±5% 1/4 W
Potentiometers	±20%

1.5 5.25 INCH MPI PLL DATA SEPARATOR DRAWINGS

ITEM NO.		DRAWING NO.	DESCRIPTION	REMARKS
1	OD	77690010-2	D SCH 5.25 MPI PLL D.S.	
2	OD	77690020-1	D PWB 5.25 MPI PLL D.S.	
5	1A	15158600-5	P. I.C. 74S112	
6	1C	15125501-5	A IC OP-AMP	
7	1A	15164400-2	P I.C. 26S02	
8	1	15105700-7	P I.C. MC4024	
9	1A	66299099-3	P I.C. 7400	
10	1A	94372606-7	P RES VARI 20% 10K	
11	1A	94372608-3	P RES VARI 20% 50K	
12	1A	77835186-6	P TRANSISTOR 2N2907A	
13	1A	75722200-5	P TRANSISTOR 2N2222A	
14	1A	94356324-7	P INDUCTOR 10 UH	
15	1	24500353-4	P CAP 10V 20% 33UF	
16	1	24504369-0	P CAP 15V 20% 10UF	
17	1	92496227-7	P CAP 100V 20% .01UF	
18	1A	94227253-5	P CAP 100V 2% 1300	
19	1C	94354817-2	P CAP 50V 20% .47UF	
20	1A	94227227-9	P CAP 300V 2% 110	
21	1C	94354804-0	P CAP 50V 20% .047UF	
22	1C	94354806-5	P CAP 50V 20% .10UF	
23	1A	94240407-0	P CAP 50V 10% 220	
24	1C	50240108-6	P VOLT REG 6.2V 5%	
25	1C	50240107-8	P VOLT REG 5.6V 5%	
26	1C	94853604-0	P DIODE SILICON 1N9148	
27	1A	24500149-0	P RES 1/2W 5% 270	
28	1A	24500144-1	P RES 1/2W 5% 160	
29	1	94360214-4	P RES 1/4W 1% 140	
30	1	94360287-0	P RES 1/4W 1% 806	
31	1A	94402164-1	P RES 1/4W 5% 2.2K	
32	1	94360352-2	P RES 1/4W 1% 3.48K	
33	1A	94360400-9	P RES 1/4W 1% 10.0K	
34	1	94360304-3	P RES 1/4W 1% 1.10K	
35	1A	94402158-3	P RES 1/4W 5% 1.2K	
36	1A	94402156-7	P RES 1/4W 5% 1K	
37	1A	94402173-2	P RES 1/4W 5% 5.1K	
38	1A	94402180-7	P RES 1/4W 5% 10K	
39	1C	92496215-2	P CAP 100V 10% 1000	
40	1C	94392606-3	P PIN-WIRE WRAP	
41	1	94260301-0	P SOCKET 16 PIN	
42	1D	77600002-8	P RIGHT ANGLE HEADER	
43	1D	77600000-2	P RIGHT ANGLE HEADER	
44	1	83433002-9	P SHUNT ASSEMBLY	
45	1A	15146300-7	P I.C. 74LS74	



RES	PL ITEM
R1	29
R2	30
R3	11
R4	11
R5	37
R6	10
R7	31
R8	27
R9	31
R10	32
R11	33
R12	34
R13	35
R14	36
R15	28
R16	36
R17	36
R18	37
R19	38
R20	31
R21	32
R22	33
R23	34
R24	36

CAP	PL ITEM
C1	23
C2	19
C3	22
C4	21
C5	18
C6	39
C7	17
C8	17
C9	15
C10	16
C11	16
C12	17
C13	17
C14	18
C15	21
C16	22
C17	20
C18	17
C19	17
C20	—

IC	PL ITEM
U1	3,41
U2	45
U3	7
U4	5
U5	6
U6	8
U7	9
U8	5

REG	PL ITEM
VR1	24
VR2	25

CONN	PL ITEM
J1	42,43
J2	—
J3	—

TSTR	PL ITEM
Q1	12
Q2	13

IND	PL ITEM
L1	14
L2	14

DIO	PL ITEM
CR1	26
CR2	26
CR3	26

JUMPER	PL ITEM
W1	44
W2	—
W3	44

CONFIGURATION CHART	
OPTION NAME	INSTALLED
MFM MODE (W1)	YES
PASS COMPOSITE DATA (W2)	NO
DATA IN (W3)	YES
C20	NO

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ASSEMBLE PER 59701127, EXCEPT DELETE REQUIREMENT OF PARA 3.8.3
2. FOR SCHEMATIC SEE ITEM 1
3. MAXIMUM COMPONENT HEIGHT .320
4. △ MARK ASSY NO. IN APPROXIMATE LOCATION SHOWN PER 12A1099P1
5. DRAWING INTERPRETATION PER 43A226599
6. SOLID BAND ON DIODES AND VOLTAGE REGULATORS INDICATE CATHODE END
7. △ OPTIONAL C20 CAN BE USED TO CHANGE DATA OUT PULSE WIDTH. IF C20 IS INSTALLED NRZ DATA OUT IS NO LONGER VALID. 22 PF GIVE 80 NSEC. 47 PF GIVES 150 NSEC, 150 PF GIVES 300 NSEC.

FIGURE 1-6. PWB (SHEET 1 OF 3)

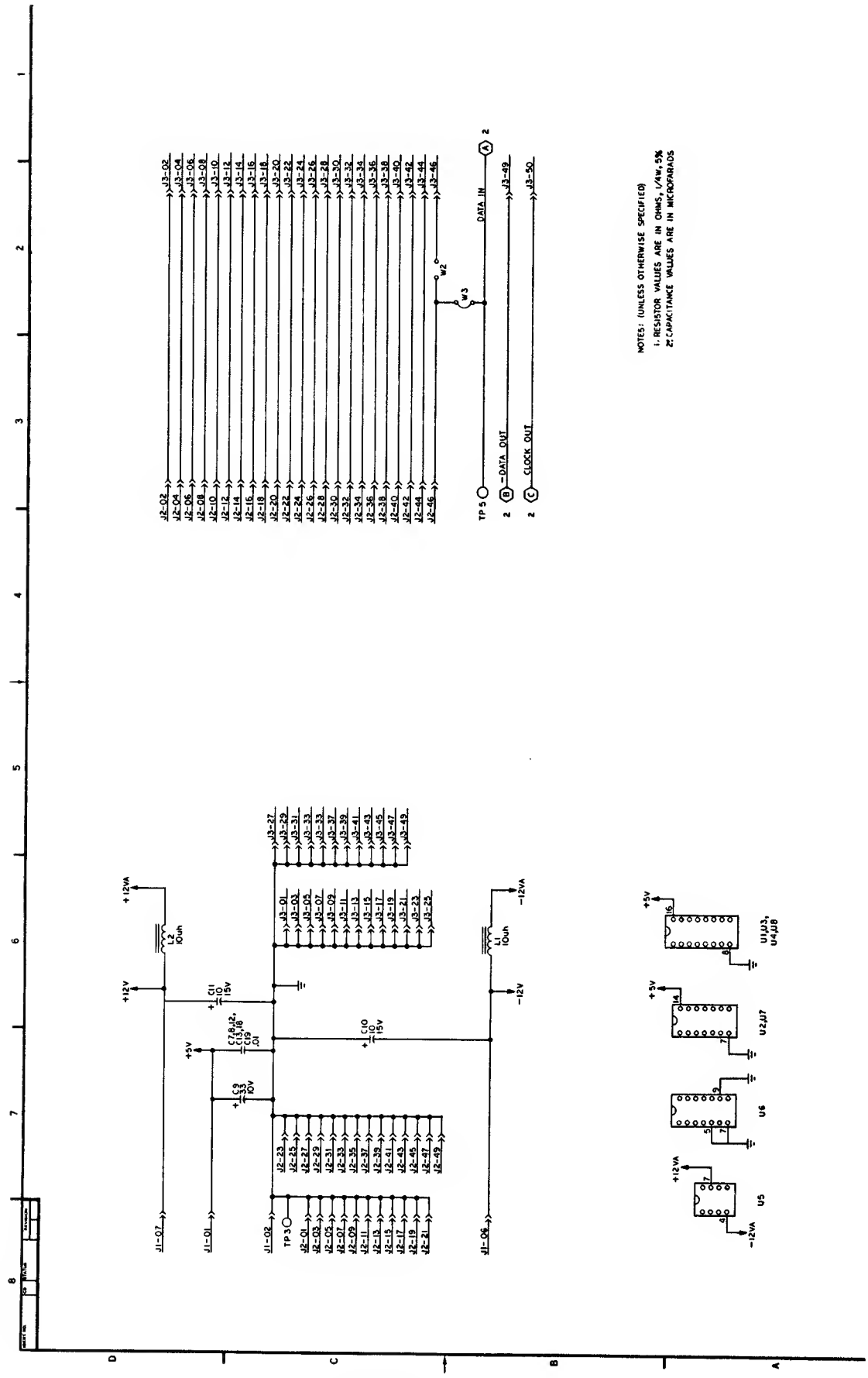


FIGURE 1-6. SCHEMATIC (SHEET 2 OF 3)

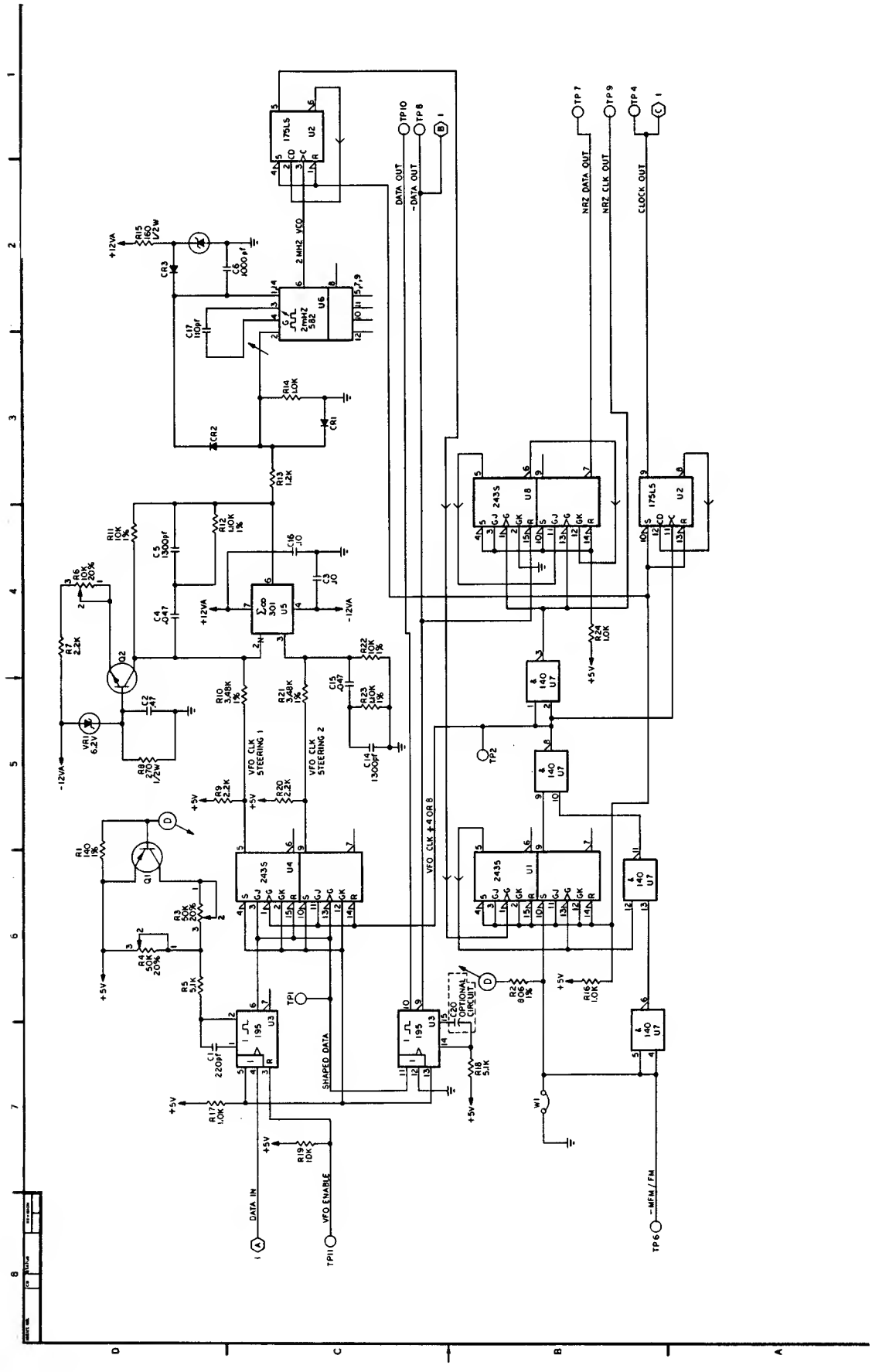


FIGURE 1-6. SCHEMATIC (SHEET 3 OF 3)

1.6 PLO CIRCUIT TEST POINTS AND ADJUSTMENTS

Adjustments to the phase lock loop after initial alignment will seldom be required. If data recovery errors become excessive, an investigation of the phase lock loop operation as described below may help pinpoint the problem.

Procedure for Alignment of the Phase Lock Loop

Equipment needed: Oscilloscope, Diskette with all ones or use header area of preformatted all ones or all zeroes.

1. Connect Channel A of the oscilloscope to TP1, output of composite read data and clock one shot, and set the horizontal sensitivity to 1 μs/div and the vertical sensitivity to about 5 volts/div. After loading the head and selecting FM make sure that data is displayed on Channel A. See Figure 1-7. Connect Channel B of the oscilloscope to TP2, output of VFO clock divide by 4 or 8. Synchronize oscilloscope on Channel A. Use all ones pattern.

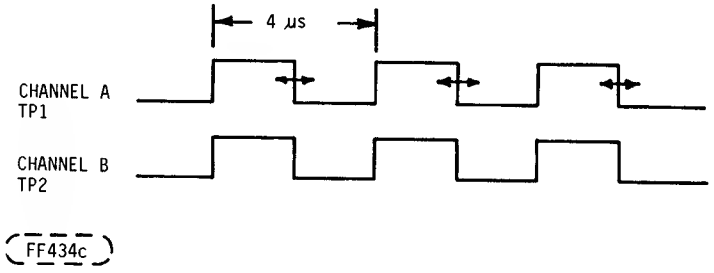


FIGURE 1-7. DATA TP1 AND VCO TP2 COMPARED

2. Adjust R4 for 4 μs pulses on Channel A. Adjust R5 for the waveform on Channel B to be as shown in Figure 1-7. With the oscilloscope controls invert Channel B and add the two channels. The oscilloscope display should be as in Figure 1-8.

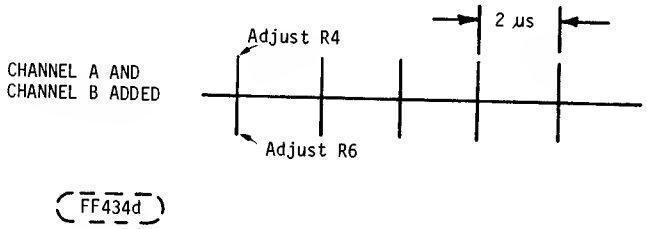
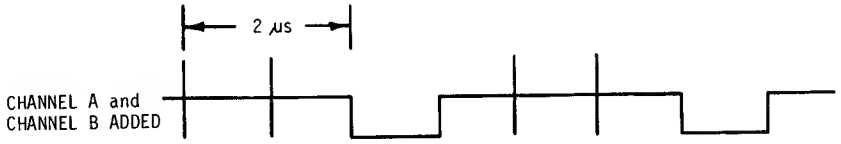


FIGURE 1-8. PHASE DIFFERENCE BETWEEN FM DATA TP1 AND VCO TP2

3. Minimize the width of the spikes of the added signal shown in Figure 1-8 by adjusting R4 and R6.

4. Select MFM operation and change the oscilloscope horizontal sensitivity to 1 μs per division.

5. Adjust R3 for the display shown in Figure 1-9.



FF433c

FIGURE 1-9. PHASE DIFFERENCE BETWEEN MFM DATA TP1 AND VCO TP2

1.7 TROUBLESHOOTING

If after aligning the PLO in accordance with the test procedure, you are still unable to recover data properly or if you are unable to align the PLO properly there are several possible sources of error.

1. If the proper filter components are not used, the DC supply may not be stable enough in terms of fluctuations or ripple content to insure stable operation of the VCO. Verify proper supply and filtering.

2. This circuit has not been proven reliable in wire wrap construction. The DC ground plane around the analog portion of the circuit is essential for the recovery rates specified. Without the ground plane the alingment can be done but the circuit is very sensitive to external noise which results in false data and clock pulses. Use DC ground plane in construction.

3. If the output of the 2 MHz free running VCO is not a clean square wave the circuit cannot be aligned and distorted clock and data pulses will be output. The source of the problem may be: 1. Filter capacitors C9, C10, or C11 breaking down - check and replace if necessary; 2. MC4024 Dual Voltage Controlled Multivibrator may be defective - replace; 3. Capacitor C17 may not be correct tolerance or may be defective - replace.

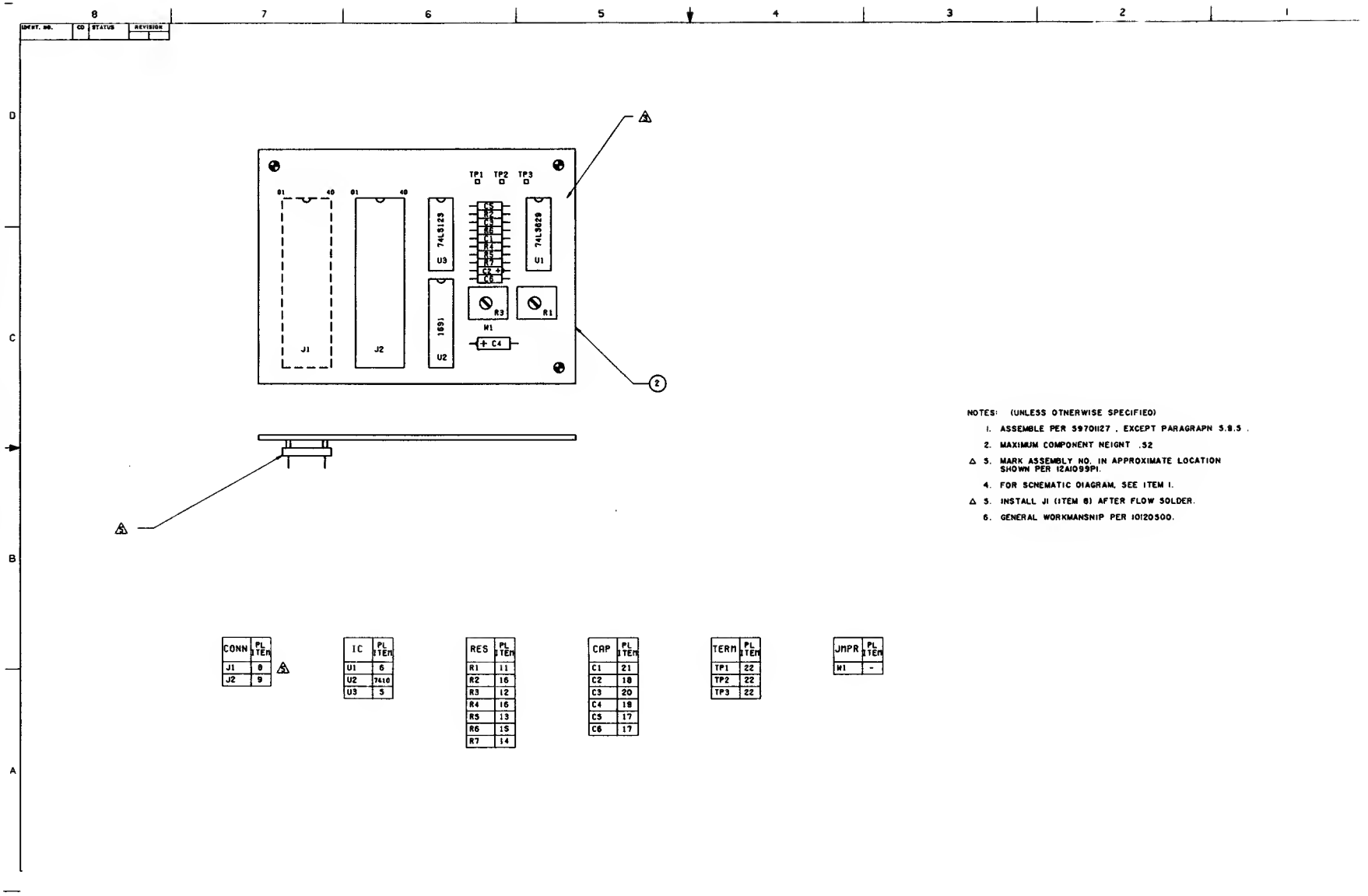
4. If steps 4 and 5 of the alignment procedure do not produce the desired waveform as shown in Figure 8, the proper chip, U3, or tolerance of capacitor C1 may be wrong. The one shot called out is a 26S05 for which the 96S02 is often substituted. If the 96S02 is used, the value of C1 should be 100 pF for proper alignment. This change would also affect the value of C20 if it is used. See the vendor data sheets for selecting proper value.

5. If C20 is used to condition the "data out" output, the "NRZ data" output may not be valid. If the "NRZ data" output is being used, verify that C20 is not installed.

6. Although we have found no problem in normal usage and testing, the PLO has a problem at the extreme ranges on spindle speed variation. If the format is written at the +3.7% extreme and the data is written at the -3.5% extreme of the nominal 300 RPM, the PLO will not synchronize.

1.8 DRAWINGS FOR THE IMPLEMENTATION OF THE WD1691 FOR THE WD179X SERIES CONTROLLERS

ITEM NO.	DRAWING NO.	DESCRIPTION	REMARKS
0001	77712510-5	D SCH, PLO-179X	
0002	77712520-4	P PWB, PLO-179X	
0005	15163422-7	P IC, 74LS123	
0008	94348010-3	P PLUG-DISCRETE	
0009	94260309-3	P SOCKET 40 PIN	
0010	94260310-1	P SOCKET 20 PIN	
0011	94372608-3	P RES VARI 20% 50K	
0012	94372610-9	P RES VARI 20% 100K	
0013	94402128-6	P RES 1/4W 5% 68	
0014	94402156-7	P RES 1/4W 5% 1K	
0015	94402175-7	P RES 1/4W 5% 6.2K	
0016	94402196-8	P RES 1/4W 5% 47K	
0017	15164019-0	P CAP 50V 20% .01UF	
0018	15164135-4	P CAP 25V 10% .68VF+	
0019	24504346-8	P CAP 10V 20% 4.7UF+	
0020	94240417-9	P CAP 50V 10% 33	
0021	94240403-9	P CAP 50V 10% 68	
0022	77670541-0	P PIN	



CONN	PL ITEM
J1	8
J2	9

IC	PL ITEM
U1	6
U2	7410
U3	5

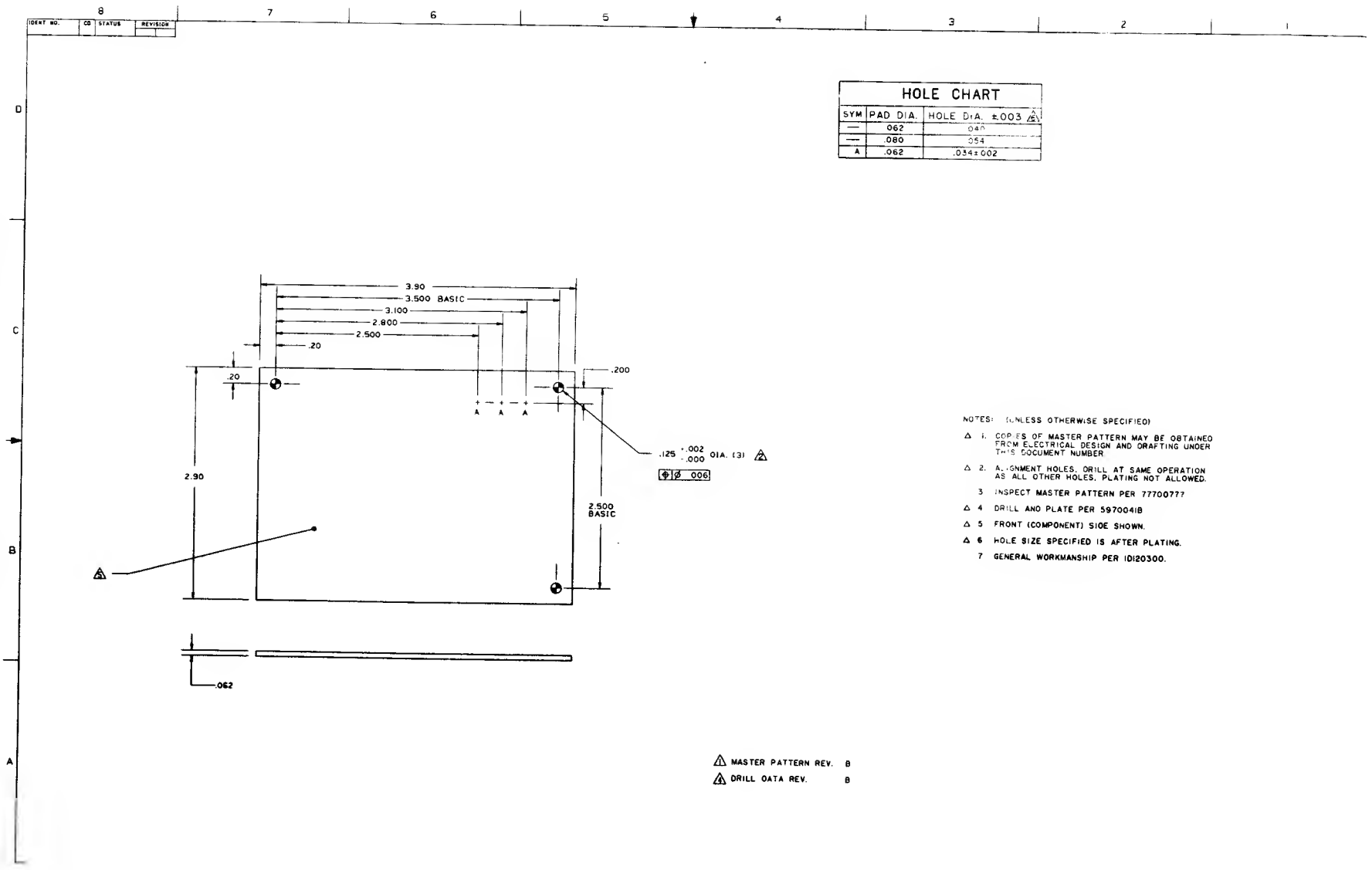
RES	PL ITEM
R1	11
R2	16
R3	12
R4	16
R5	13
R6	15
R7	14

CAP	PL ITEM
C1	21
C2	18
C3	20
C4	18
C5	17
C6	17

TERM	PL ITEM
TP1	22
TP2	22
TP3	22

JMPR	PL ITEM
M1	-

FIGURE 1-10. PWB (SHEET 1 OF 3)



HOLE CHART		
SYM	PAD DIA.	HOLE DIA. ±.003
—	.062	.040
—	.080	.054
A	.062	.034±.002

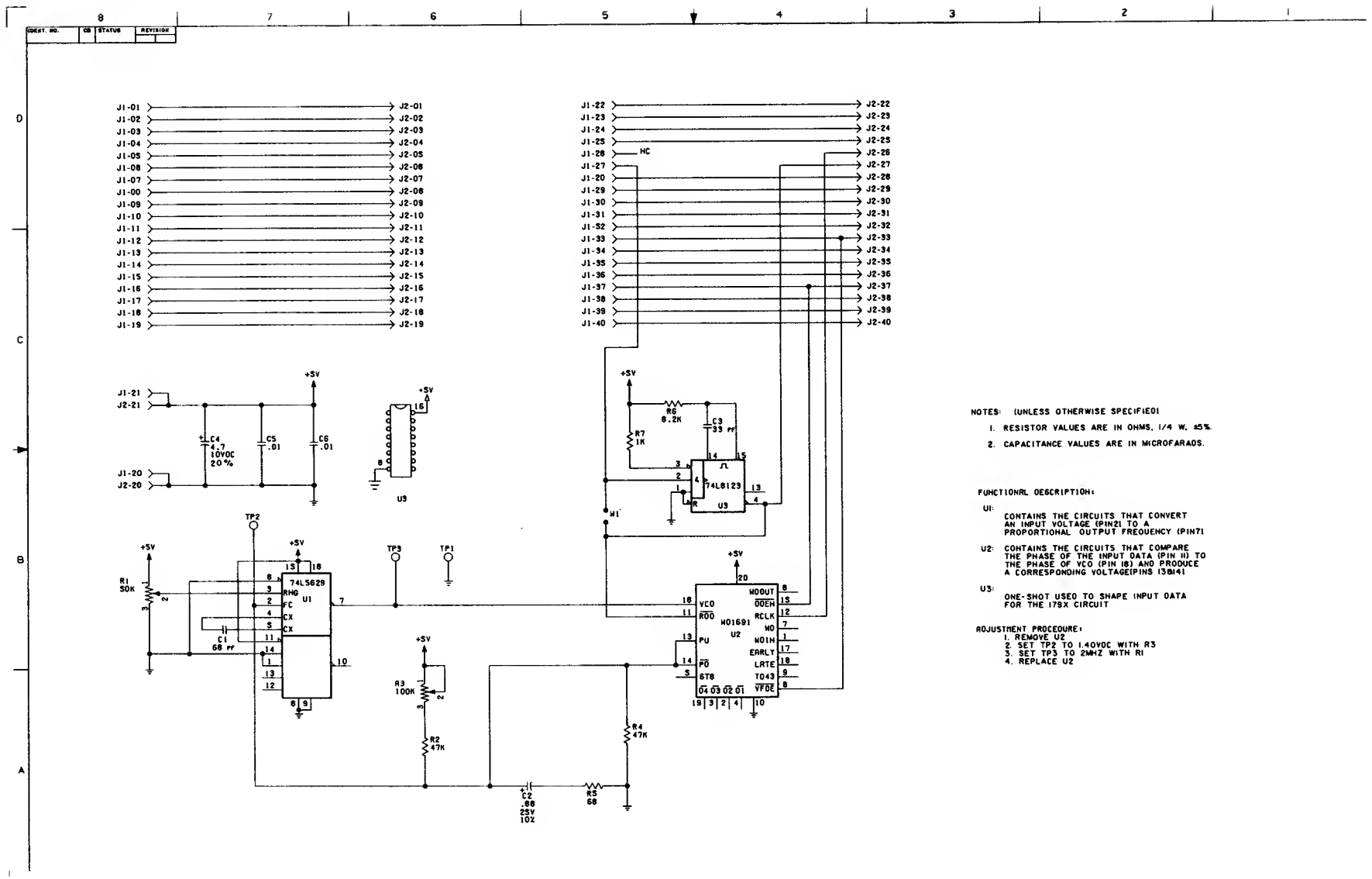
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COPIES OF MASTER PATTERN MAY BE OBTAINED FROM ELECTRICAL DESIGN AND DRAFTING UNDER THIS DOCUMENT NUMBER.
2. ALIGNMENT HOLES, DRILL AT SAME OPERATION AS ALL OTHER HOLES, PLATING NOT ALLOWED.
3. INSPECT MASTER PATTERN PER 77700777
4. DRILL AND PLATE PER 5970041B
5. FRONT (COMPONENT) SIDE SHOWN.
6. HOLE SIZE SPECIFIED IS AFTER PLATING.
7. GENERAL WORKMANSHIP PER IDI20300.

1 MASTER PATTERN REV. B

2 DRILL DATA REV. B

FIGURE 1-10. PWB (SHEET 2 OF 3)



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTOR VALUES ARE IN OHMS, 1/4 W, ±5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.

FUNCTIONAL DESCRIPTION:

U1: CONTAINS THE CIRCUITS THAT CONVERT AN INPUT VOLTAGE (PIN2) TO A PROPORTIONAL OUTPUT FREQUENCY (PIN7)

U2: CONTAINS THE CIRCUITS THAT COMPARE THE PHASE OF THE INPUT DATA (PIN 11) TO THE PHASE OF VCO (PIN 16) AND PRODUCE A CORRESPONDING VOLTAGE(PINS 13&14)

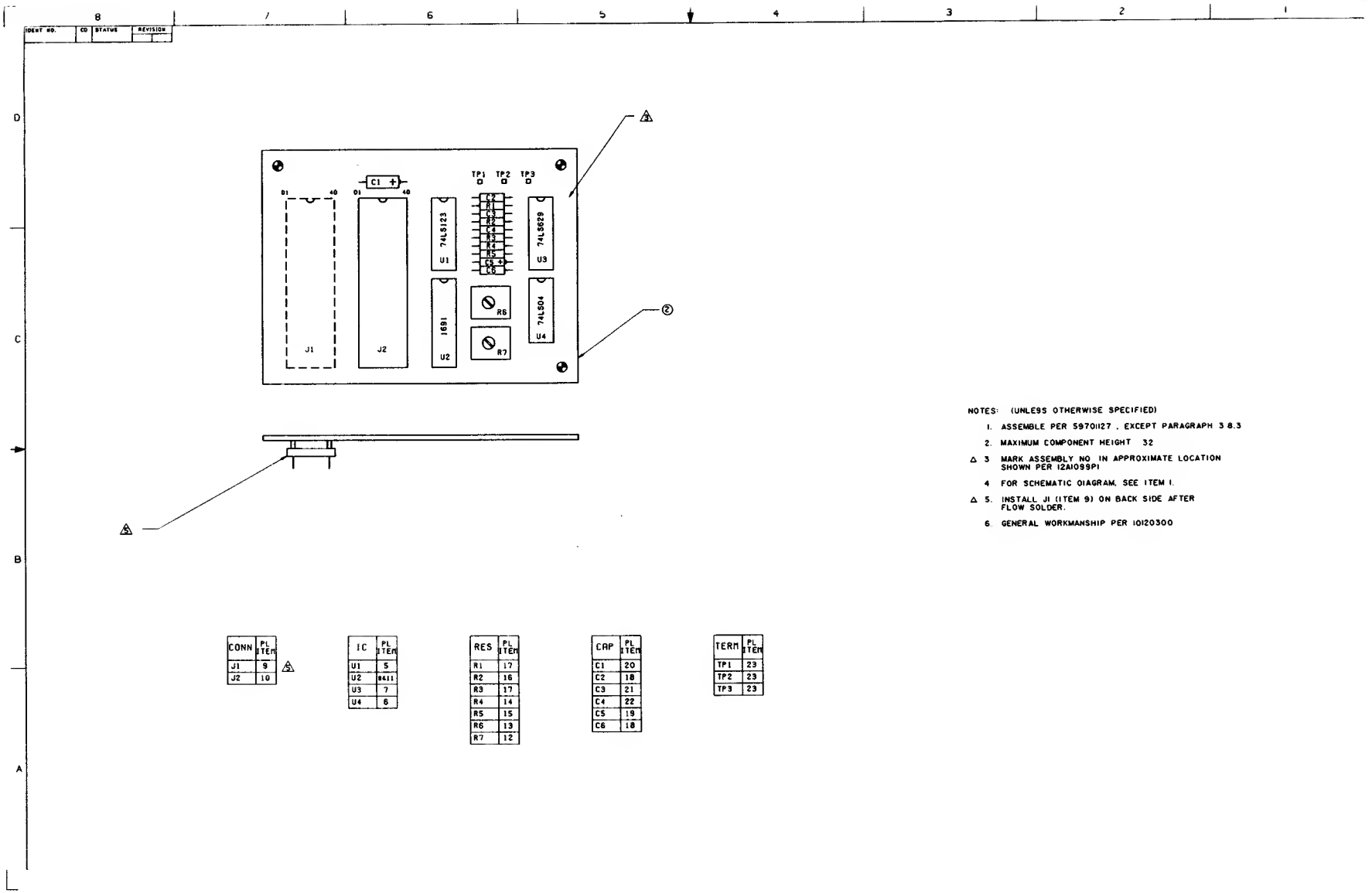
U3: ONE-SHOT USED TO SHAPE INPUT DATA FOR THE 179X CIRCUIT

ADJUSTMENT PROCEDURE:
1. REMOVE U2
2. SET TP2 TO 1.40VDC WITH R3
3. SET TP3 TO 2MHZ WITH R1
4. REPLACE U2

FIGURE 1-10. SCHEMATIC (SHEET 3 OF 3)

1.9 DRAWINGS FOR IMPLEMENTATION OF THE WD1691 FOR THE NEC765 AND COMPATIBLE CONTROLLERS

ITEM NO.		DRAWING NO.	DESCRIPTION	REMARKS
1	OD	77713160-8	D SCH, 765 DATA CONTROL	
2	OD	77713170-7	P PWB, 765 DATA CONTROL	
5	1A	15163422-7	P IC, 74LS123	
6	1A	15145100-2	P I.C. 74LS04	
7		74LS629	UNDEF. ON ID	
8		WD1691	UNDEF. on ID	
9	1A	94348010-3	P PLUG-DISCRETE	
10	1C	94260309-3	P SOCKET 40 PIN	
11	1C	94260310-1	P SOCKET 20 PIN	
12	1A	94372608-3	P RES VARI 20% 50K	
13	1A	94372610-9	P RES VARI 20% 100K	
14	1A	94402128-6	P RES 1/4W 5% 68	
15	1A	94402156-7	P RES 1/4W 5% 1K	
16	1A	94402175-7	P RES 1/4W 5% 6.2K	
17	1A	94402196-3	P RES 1/4W 5% 47K	
18	1A	15164019-0	P CAP 50V 20% .01UF	
19	1A	15164135-4	P CAP 25V 10% .68VF+	
20	1C	24504346-8	P CAP 10V 20% 4.7UF+	
21	1A	94240417-9	P CAP 50V 10% 33	
22	1A	94240403-9	P CAP 50V 10% 68	
23	1C	94392600-6	P PIN-WIRE WRAP	



CONN	PL ITEM
J1	9
J2	10

IC	PL ITEM
U1	5
U2	8411
U3	7
U4	6

RES	PL ITEM
R1	17
R2	16
R3	17
R4	14
R5	15
R6	13
R7	12

CAP	PL ITEM
C1	20
C2	18
C3	21
C4	22
C5	19
C6	18

TERM	PL ITEM
TP1	23
TP2	23
TP3	23

FIGURE 1-11. PWB (SHEET 1 OF 3)

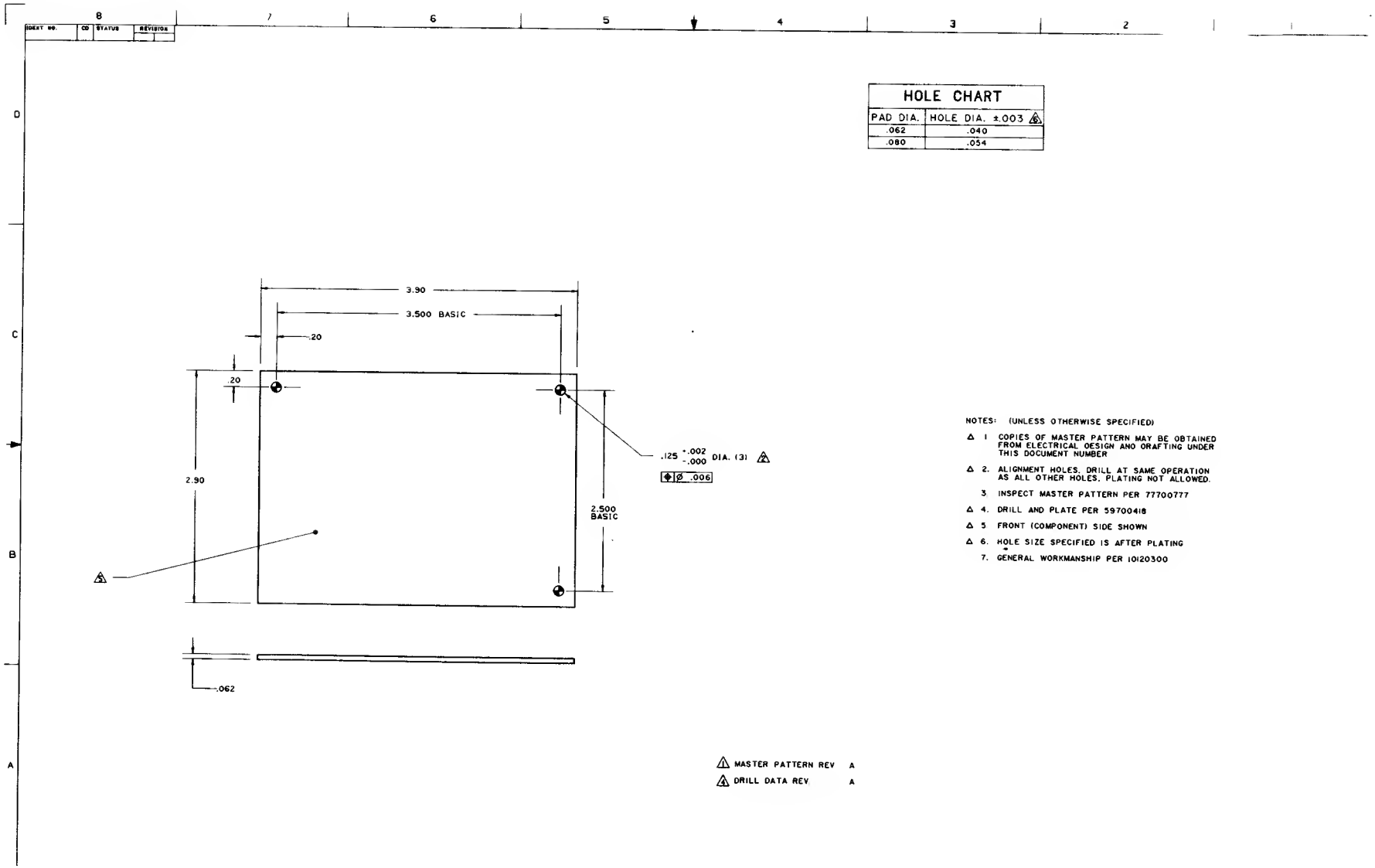
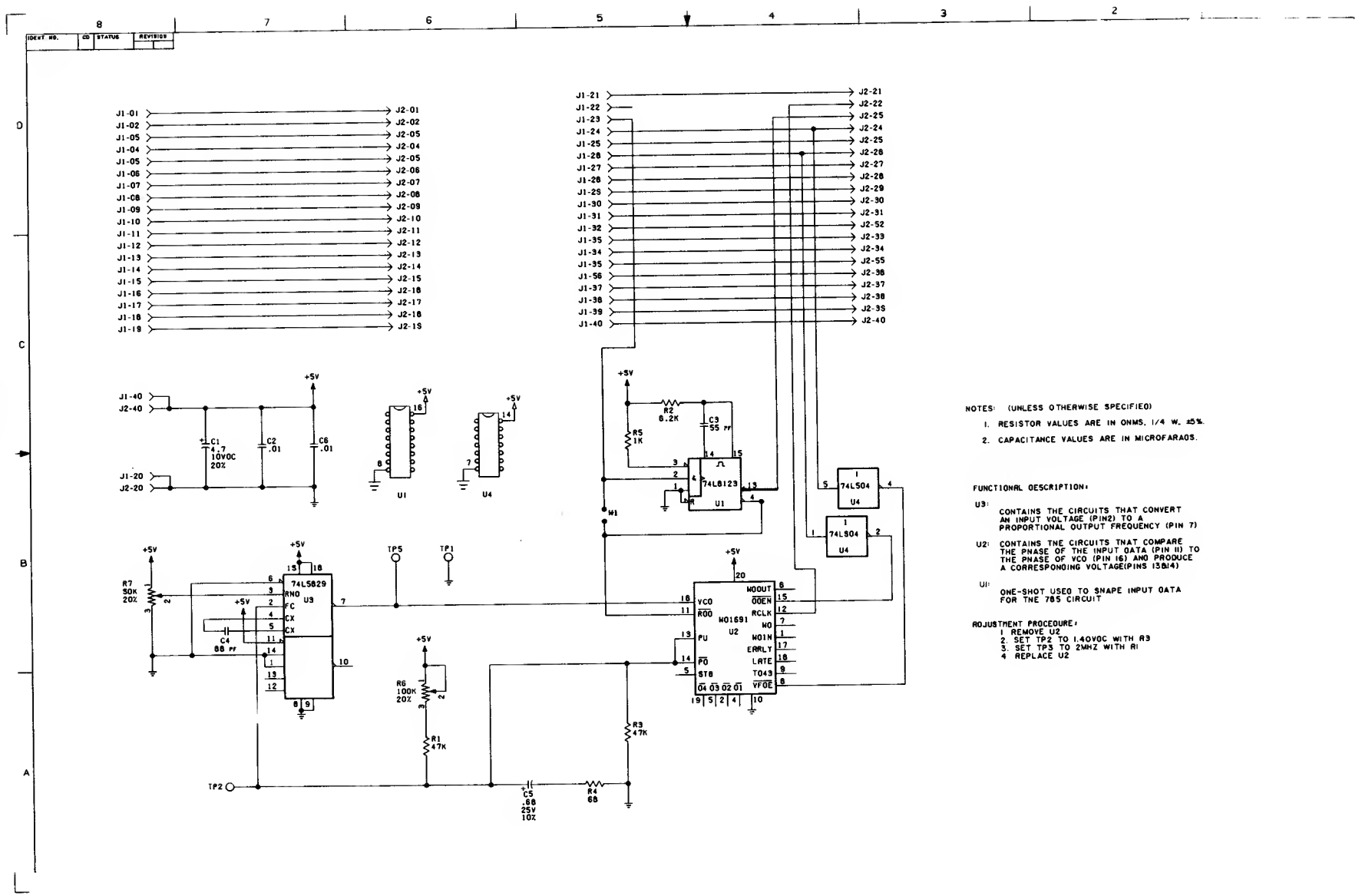


FIGURE 1-11. PWB (SHEET 2 OF 3)



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTOR VALUES ARE IN OHMS, 1/4 W, ±5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.

FUNCTIONAL DESCRIPTION:

U3: CONTAINS THE CIRCUITS THAT CONVERT AN INPUT VOLTAGE (PIN2) TO A PROPORTIONAL OUTPUT FREQUENCY (PIN 7)

U2: CONTAINS THE CIRCUITS THAT COMPARE THE PHASE OF THE INPUT DATA (PIN 11) TO THE PHASE OF VCO (PIN 16) AND PRODUCE A CORRESPONDING VOLTAGE(PINS 13&14)

U1: ONE-SHOT USED TO SHAPE INPUT DATA FOR THE 785 CIRCUIT

ADJUSTMENT PROCEDURE:
1. REMOVE U2
2. SET TP2 TO 1.40VDC WITH R3
3. SET TP3 TO 2MHZ WITH R1
4. REPLACE U2

FIGURE 1-11. SCHEMATIC (SHEET 3 OF 3)

1.10 APPLICATION NOTES

The basic PLO circuit has been applied and tested with the Western Digital 179X and NEC 765 LSI controllers used for 8 inch Flexible Disk Drives and has been used in existing CDC labs and previous products. There are existing application notes for applying the PLO to 8 inch drives. Refer to the following documents.

1. Application Note: Interfacing CDC 9404 and 9406 series Flexible Disk Drives to the Western Digital 179X controller P/N 75897549.

2. Application Note: Considerations for interfacing the NEC 765 controller to the CDC 9404B and 9406-2/3 Flexible Disk Drives. P/N 77641943.

To apply a PLO to the 5.25 inch flexible disk drive controllers one should consult the manufacturers data sheets on controllers and controller chips.

If the PLO described in Section 5 is used to precondition data and generate the synchronous clock, the following circuit modifications may be necessary.

1. If using the NEC 765 LSI controller the Data Out output of the PLO becomes the RDD (read data input) to the controller chip and Clock Out becomes the RDW input. In order to have the proper data pulse width C20 will have to be selected and installed in the circuit. Using the 26S02 one shot, C20 should be selected so the Data Out pulse width is 160 nanoseconds. C20 should be 47 to 57 pF. Installing this capacitor will invalidate the NRZ Data Out output of the PLO.

2. If using the Western Digital 179X LSI controller the Data Out output of the PLO becomes the Raw Data input of the 179X chip. This requires a preconditioned data pulse width of 300 nanosecond. C20 of 100 pF can be installed to accomplish this.

3. Values given for C20 are for 5.25 inch FDD.

Contact your CDC Salesperson, Applications Engineering, or Literature Distribution Service for Application Notes.

2.1 OPERATION OF SYNCHRONOUS COUNTER DATA RECOVERY CIRCUITS

Refer to Figures 2-1 and 2-2.

VCO Sync (1) is derived by the Controller from input data. When VCO Sync is low it forces the elements of the synchronous counter circuit to a known initial condition. When VCO Sync is high indicating the presence of data the circuit is permitted to run.

A positive going transition of inverted raw read data (2) toggles FF "A" causing the data input of FF "B" (3) to go high. The next positive going transition of the 8 MHz (4 MHz for FM operation) clock sets FF "B". Shaped Read Data (5) goes high. Inverted read data (6) goes low resetting FF "A", disabling G1 (count) and enabling preload of a four bit binary counter. The following positive clock transition resets FF "B" and preloads the four bit counter. Shaped Read Data (5) goes low terminating a 125 ns positive going pulse. The Shaped Read Data pulse always has a duration of 125 ns (the interval between 8 MHz pulses) but its leading edge lages the raw read data transition by an unpredictable value which may be as much as 125 ns.

Each succeeding positive transition of the 8 MHz clock increments the four bit counter. After eight counts are accumulated (1 μs) the most significant bit of the counter (7) goes high, toggling FF "C". In the absence of further read data pulses, the counter output (7) will produce a positive transition after every sixteen clock pulses, toggling FF "C" at 2 μs intervals. Each time a data pulse occurs the counter will be resynchronized to center the data pulse between transitions of the data window.

For bit to bit spacing, the preload derived from the data pulse becomes the center of the data cell. The time between the leading edge of the data pulse and the trailing of the current data window is always one microsecond.

If the bit to bit spacing is always greater than three and less than five microseconds each succeeding data pulse will fall within a data window and the synchronous counter data recovery scheme will work reliably.

However, the sum of all the factors producing bit shift (thus reducing the data window) is often more than 1000 nanoseconds. If bit shift exceeds 1000 nanoseconds, the succeeding data pulse will fall outside the data window and synchronization of clock and data pulses is lost. Synchronization cannot be regained until the next VCO Sync enable occurs.

2.2 PROBLEMS WITH SYNCHRONOUS COUNTER DATA RECOVERY CIRCUITS

NEC Application Note #8 describes a typical synchronous counter data recovery circuit. The circuit is said to work reliably when used to recover single density (FM) data from either an 8 inch or 5.25 inch floppy diskette. However, the user is cautioned not to use the circuit to attempt to recover MFM data from an 8 inch drive in which a bit shift of 500 nanoseconds or more may occur.

This section discusses several factors which make the synchronous counter data recovery circuit unsuitable for such use.

1. Bit Shift at Inner Tracks

   Bit Shift at the inner tracks is typically 800 to 1200 nanoseconds with stand alone drives and medium resolution media.

2. Setup and Hole Time

   The NEC765/INTEL8272 controller chips require 70 nanoseconds setup and hold time.

3. Clock Frequency

   To achieve ±125 nanosecond data pulse position resolution an 8 MHz counter clock frequency is required. Four MHz provides only ±250 nanosecond resolution and so on.

4. Random Bit Shift

   The following factors contribute to random bit shift:
   a. Resolution of the media (low to high) typically contributes ±200 nanoseconds jitter.

   b. Electromagnetic noise, through radiation or conduction, from switching power supplies, flyback transformers, etc., typically contribute 200 to 500 nanoseconds jitter. Worst case contributions from this source may be as high as 600 to 800 nanoseconds jitter.

5. Write Precompensation

   Correctly implemented write precompensation, with a value of 250 nanoseconds, can reduce bit shift values. Values in the range 800 to 1200 nanoseconds may be reduced to the 600 to 1000 nanosecond range.

6. Other Factors

   Other factors which may contribute to random bit shift are:
   a. Clock jitter
   b. Bit assymetry
   c. Disk speed variations

   These factors combined may reduce the data recovery window by 100 nanoseconds.

   The MFM bit cell time for the 5.25 inch floppy is 4 microseconds with a useable data window of 2 microseconds. All bit shift factors decrease time available for the data window. Typical values (in nanoseconds) are:

	Without Precompensation	250 Nanoseconds Precompensation
Data Window	2000	2000
Average Bit Shift	1000	800
RFI/EMI	200	200
8 MHz Clock Resolution	125	125
Average Media Variations	100	100
Jitter/Asymmetry/Speed	100	100
Controller Setup	70	70
	1595	1595
Data Window Margin	405	605

Worst case conditions could reduce the data window margin by an additional 200 to 300 nanoseconds.

Any data recovery scheme must be able to track bit jitter or bit shift in a range of ±800 nanoseconds to have any data window margin for worst case conditions, whether or not precompensation is used when the data is written. At present, only the analog phase locked loop has the ability to handle the actual bit shift range requirements.

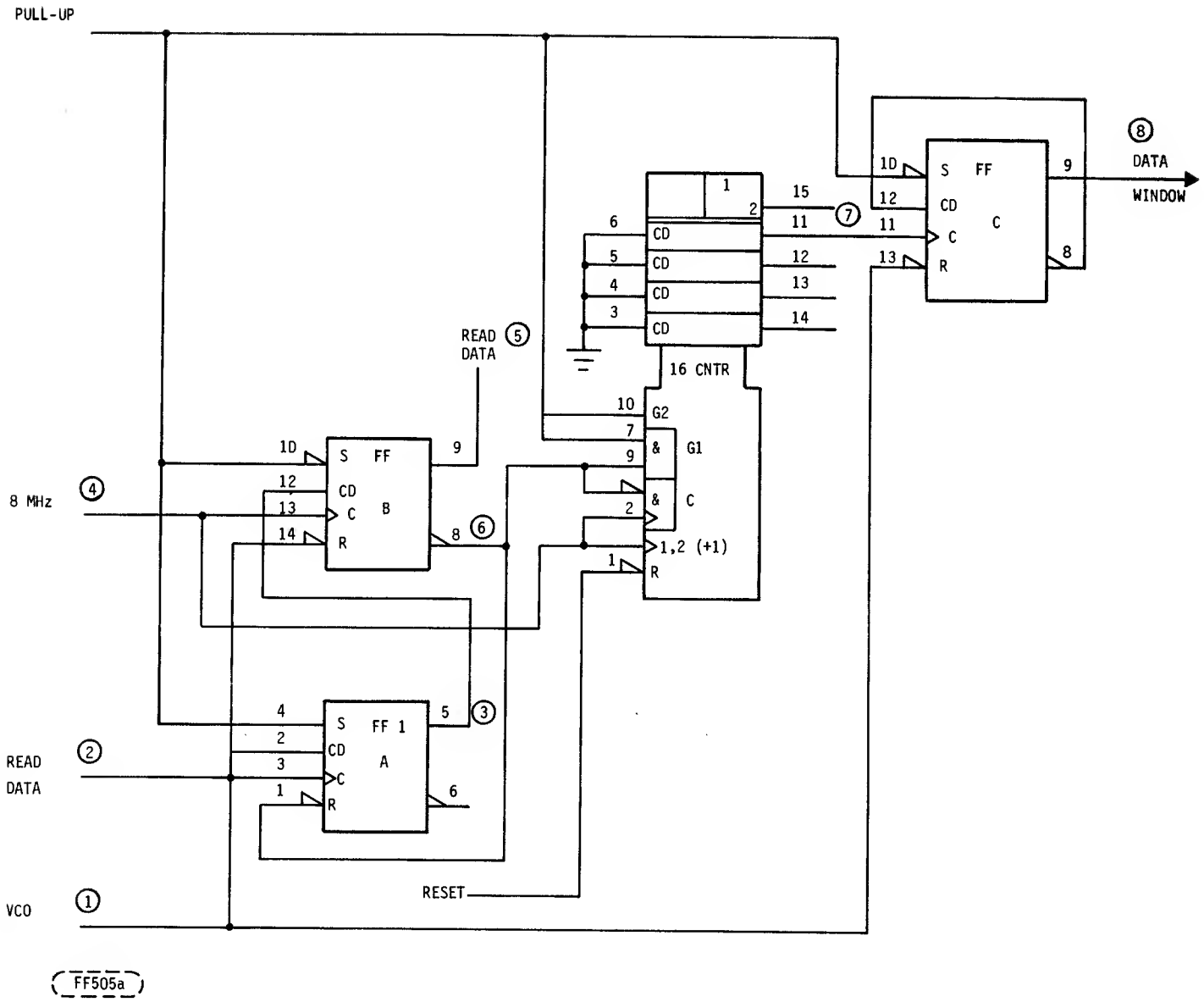


FIGURE 2-1. SYNCHRONOUS COUNTER CIRCUIT

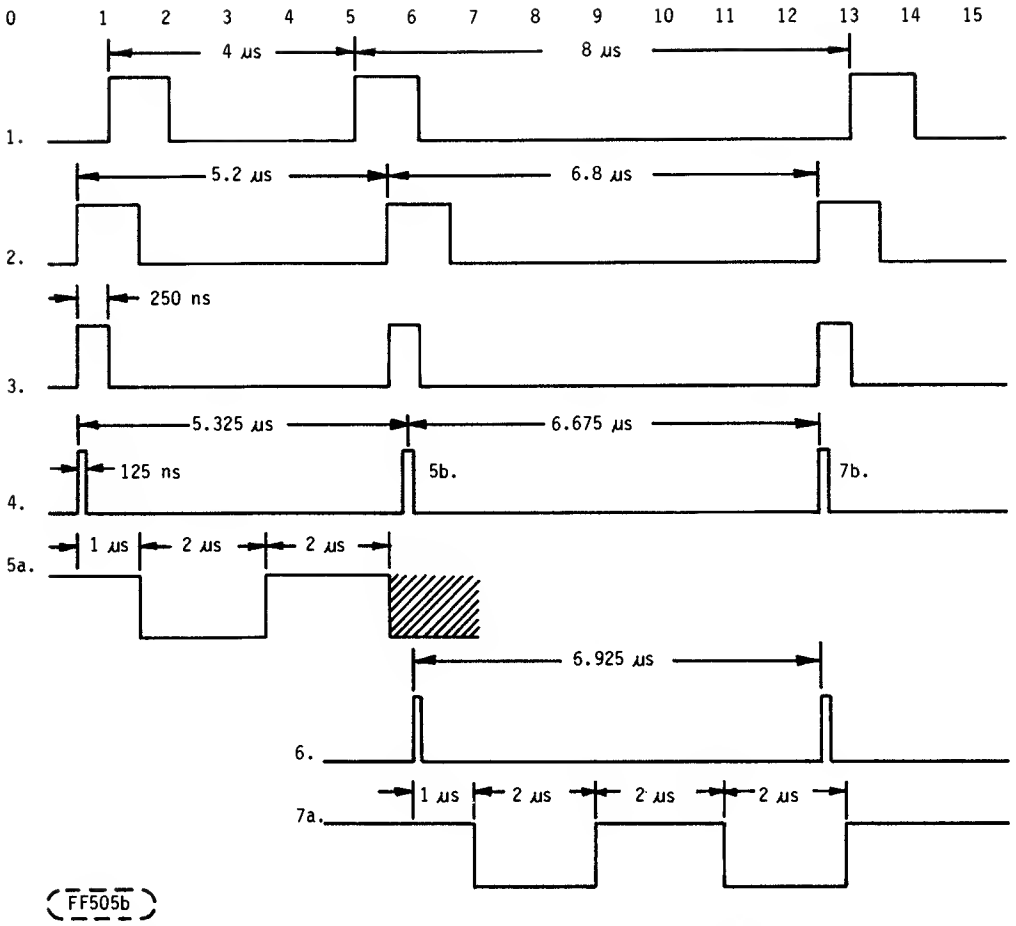


FIGURE 2-2. SYNCHRONOUS COUNTER TIMING DIAGRAM

3.1 WHY WE NEED PRECOMPENSATION

There are two encoding schemes currently in use on CDC FDD's. Frequency Modulation (FM) also called double frequency (DF) or single density and modified Frequency Modulation (MFM) or double density, MFM is called double density because it doubles the data bit density while maintaining the same maximum number of flux reversals per inch. MFM encoding divides the data window, the time allowed for the bit to appear and be recognized, by two. This results in an MFM data window of two microseconds as compared to the FM data window of four microseconds. The reduced data window size makes MFM less tolerant of variations or shift in the data pulses from the nominal position. Adjacently recorded pulses interact as they are written and when read appear to be shifted from the nominal position where they should occur.

The major components of the shift effect (referred to as peak shift) are predictable for given heads, media, and electronics. Due to the predictable nature of the peak shift phenomena it is possible to compensate for the shifted pulses. The recommended method of compensation is write precompensation.

In write precompensation, the data train is examined prior to its being written and compared to predetermined worst case shift patterns. In the comparison it is determined which direction each bit will shift, either early or late from the nominal position, then the bit is written late or written early, i.e., shifted in the opposite direction of the predicted shift. This compensates for the peak shift effect and causes the read back data to appear in the nominal position, thus insuring that it will be read correctly.

With MFM encoding the 5.25 inch FDD's, it is recommended that write precompensation be used on all tracks (0 through 39) when using 48 TPI drives and on tracks 43 through 79 when using 96 TPI drives. The amount of precompensation should be 250 nanoseconds.

3.2 CAUSES OF PEAK SHIFT

Peak shift is generally attributed to characteristics of the write operation and it is often referred to as the interaction of the pulses as they are written. A detailed examination can break the effect down into a number of predictable causes.

1. The action of the Read/Write windings in the write operation:
   There are definite real times for a magnetic field to build to full strength in the gap of the head as the write current is turned on, and then to collapse and decay as the write current is toggled and the flux reversed. This and the movement of the media past the head during the write operation contribute major components of the predictable peak shift. The construction of the head (materials, number of turns in coils, value of write current, etc.) determine the change and decay time intervals. As the bit density increases the decay of the field may not be complete before the current is toggled and the field reversed. This results in a peak shift

or a distortion of the written pulse. By superimposing the two fields set up by each write current toggle, a very close approximation of peak shift can be calculated by taking the algebraic sum of superimposed patterns. See Figure 3-1.

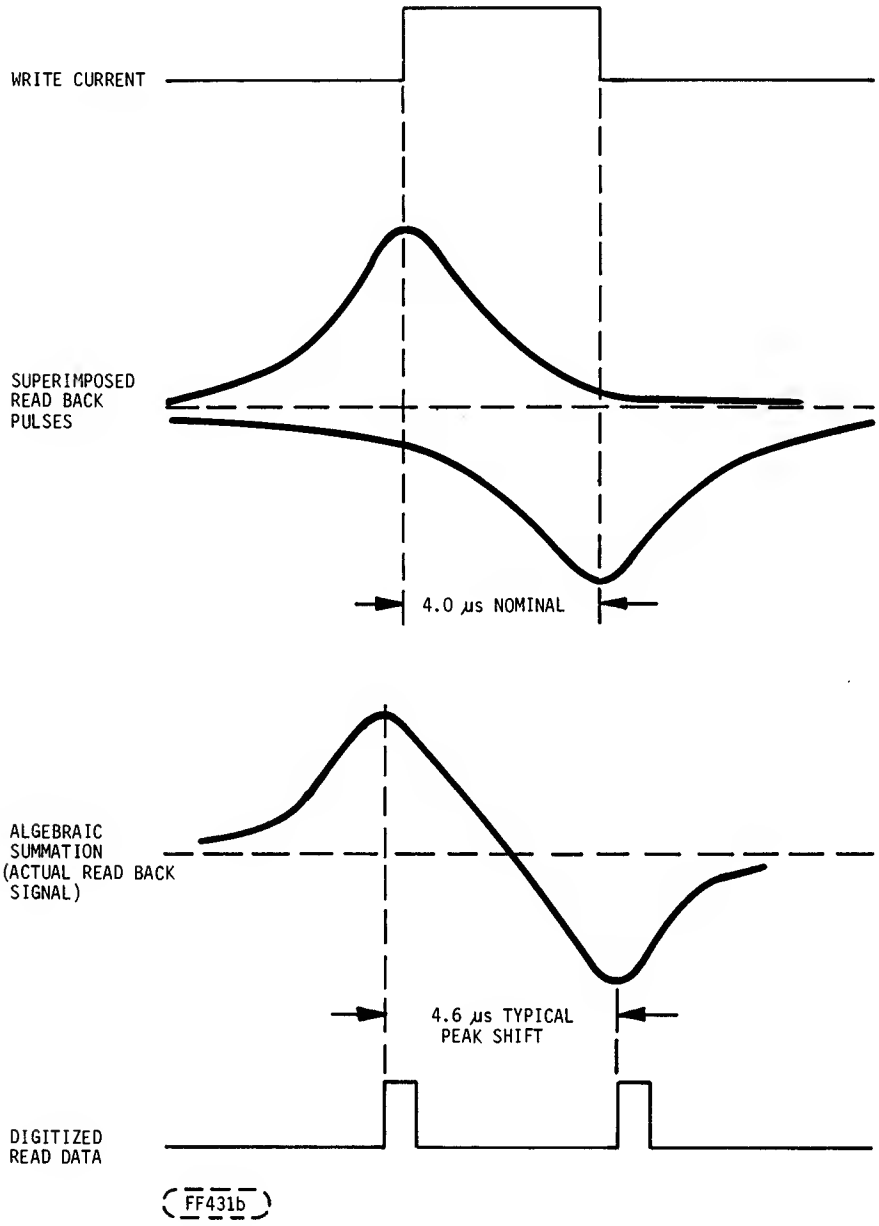


FIGURE 3-1. PEAK SHIFT DERIVATION

2. Write current level and write current rise time influnces the peak shift effect. High current levels produce faster rise time, faster saturation of core and media but longer decay time. Reducing the level of write current reduces the effect of peak shift but does not saturate as rapidly during a write and may reduce reliability.

3. The thickness of the magnetic coating on the media is directly related to the amount of peak shift.

   a. Thin coating on the media permits low write currents to be used. This allows rapid and effective saturation of the media and records the pulse with the lowest degree of peak shift. The major disadvantage of thin coatings is the tendency to wear out more quickly.

   b. A thick oxide coat has very good wear characteristics but requires a higher write current to saturate and effectively record the pulses. The higher write currents increases the peak shift problem.

   c. A balance between wear characteristics and recording reliability is the design aim. This produces an optimum thickness for long term wear and minimal shift of recorded pulses.

4. The type of erasure used in the write process can affect the degree of peak shift. A total DC erase prior to writing (pre-erase) would insure that no residual patterns of previously written data on the media would interact with the data being written to induce peak shift.

   The tunnel erase head used on CDC flexible disk drives trim erases the track data as it is written to the media providing separation bands between tracks. These separation bands minimize the influence of data stored on adjacent tracks and results in an improved signal to noise ratio.

5. The gap length of a read/write head directly relates to write current levels that must be used to create the field strength needed to saturate the media and record the pulse. A wider gap would require a higher current to maintain full strength, effectively increasing the degree of peak shift.

6. Variations in spindle speed of the drive will also cause variations in peak shift. This can be viewed as pulse jitter and phase shifting of the data pulses as they are read back.

7. The band width of the read amplifier/filter circuit can affect the amount of peak shift on the read back signal. Any phase distortion introduced by the differential amplifiers can add to the effect of peak shift when the signals are summed and used to produce the digitized version of the analog signal. A wider band width filter does not cause as much of a problem; however, a wide band width filter allows a higher degree of noise which may reduce peak shifting yet reduce overall reliability.

   The reason the read electronics affects the peak shift is that the filter characteristics respond to the changes in frequency and thus may increase or decrease the amount of peak shift.

3.3 RECOMMENDED SOLUTIONS

Peak shift degrades the read accuracy by distoring the waveform. Therefore, write precompensation is recommended to correct for this effect. This section discusses peak shift in terms of early, zero, and late peak shift and the specific patterns which require write precompensation in MFM encoding.

1. The ideal flux reversal would be instantaneous as shown in Figure 3-4. The current would immediately switch from one polarity to the other with no distortion introduced by the build up and decay of the magnetic field.

With MFM encoding techniques, adjacent data pulses are close enough to interact with one another. Because two pulses tend to have a portion of their individual signals superimposed on each other, the actual read back voltage is the algerbraic sum of the pulses.

This summation can cause a shift either to the left or right of a reference pulse in a data train. A shift to the left of the reference bit is said to be early peak shift. As it actually appears on the read back prior to the actual time it was written (in reference to the bits next to it). A late peak shift is a shift to the right of the reference bit and it appears on the read back later than it was written. An on time, or zero peak shift occurs when the read back is in the same location in the data window as it was written.

When all "1's" or all "0's" are being recorded, the data frequency is constant. The pulses are spaced apart by one cell. As a result, the pulse spacing causes the overlap errors to be equal and opposite. The negative going and positive going errors cancel each other. This is a "zero peak shift" condition.

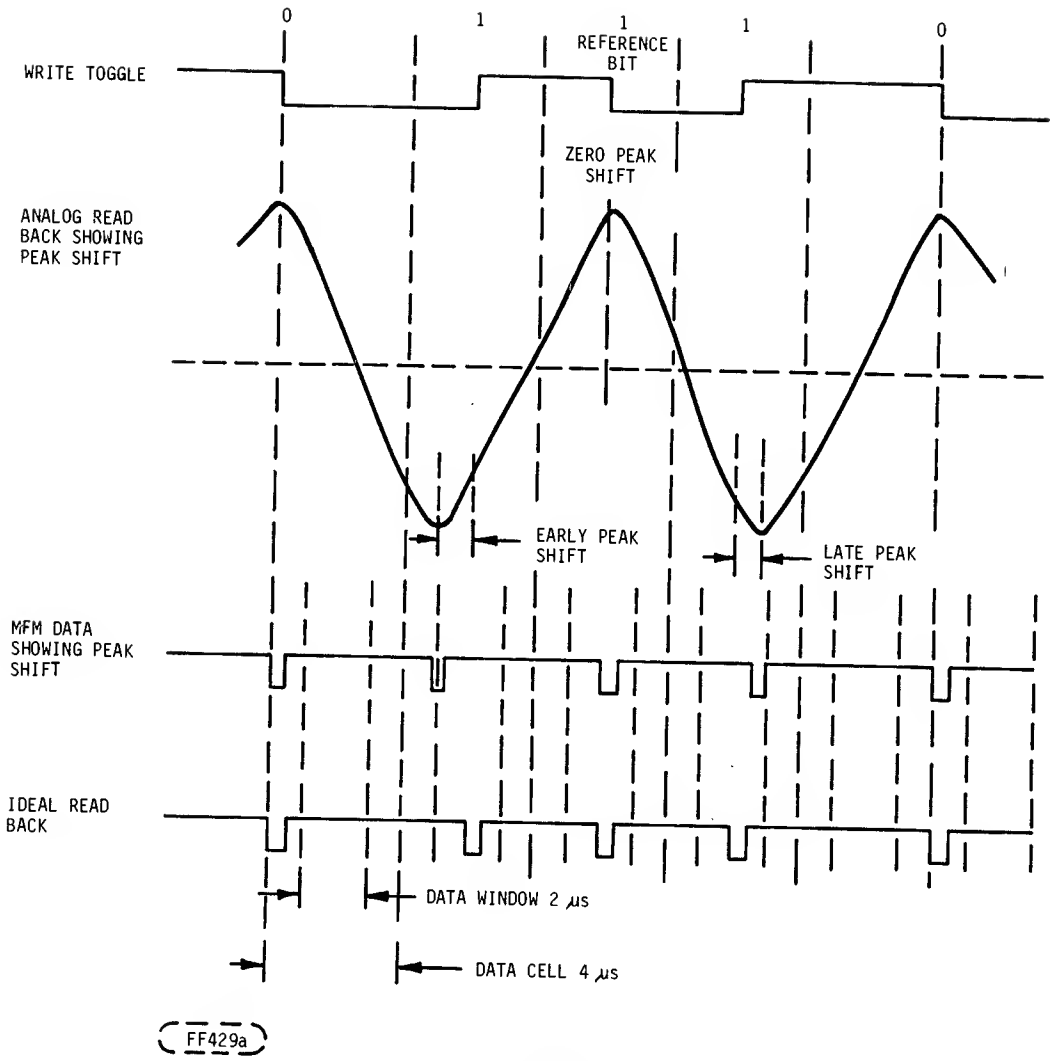


FIGURE 3-2. MFM PEAK SHIFT

Peak shift occurs when there is a change in frequency. A "011" pattern represents a frequency increase since there is a delay of about 1.5 cells between the "01" and only 1 cell between the "11". As a result, the squeezing of the cells cause the mathematical average, the actual read back voltage, to shift the apparent peak to the left. This is early peak shift.

A "110" pattern represents a frequency decrease since a pulse is not written at all in the third cell. The summation of the signals from the flux reversals going from the "11" pattern and decreasing in frequency to the "0" bit appears as a shift of the second "1" further to the right, toward the edge of the next data window. This is late peak shift.

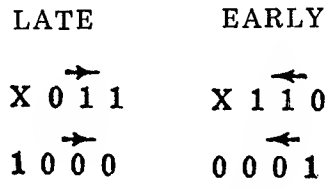
2. The write precompensation is applied to data patterns which are known to exhibit the largest peak shift. Precompensation simply shifts the data bit, in time, a pre-determined amount. The recommended amount with present heads, media, and electronics in 250 nanoseconds. Patterns known to shift

early are delayed 250 nanoseconds, bits not shifted are written on time, and bits known to shift late are written 250 nanoseconds early.

As shown in Figure 3-2, if the bit is shifted too far either early or late, it may appear at the edge of the data window and therefore not be correctly recovered. The precompensation shifts the bit back into the data window and improves read back reliability.

The data patterns which produce worst case peak shift are shown in Figure 3-3.

The following MFM patterns are compensated (bit shifted) in the direction of the arrow.



X = Don't Care

FIGURE 3-3. PEAK SHIFT WORST CASE DATA PATTERNS

Diagrams of each data pattern, showing the reference bit, the combinations which produce shift, the direction of shift, early or late, and which bit is actually shifted, are shown in Figure 3-4 thru 3-7.

Write data is shifted serially through a floating window and each pattern is compared with the above patterns. If a pattern is matched, it is decoded to generate a control level which indicates the direction of shift, early or late.

Only the bit which is indicated as "bit shifted" is precompensated. All other bits are written on time, that is they exhibit zero peak shift.

3. For optimum reliability in data recovery, a write precompensation circuit should be capable of performing in the following manner:

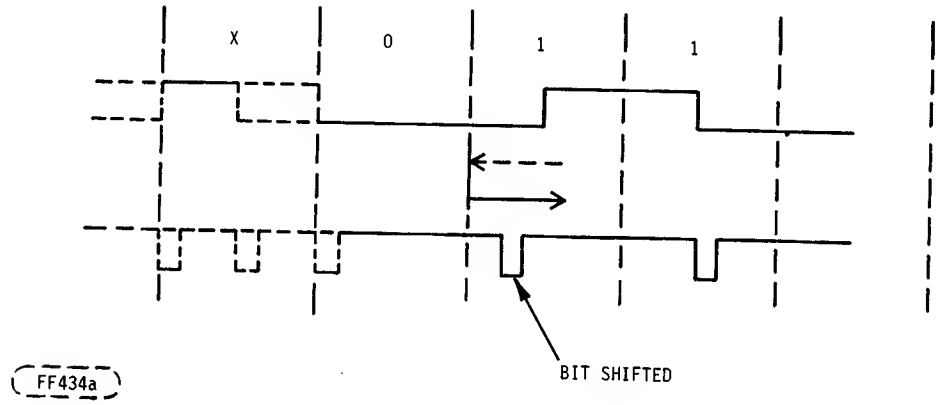
   1. The circuit should look at the data train and detect the worst case shift patterns (refer to Section 3.2).

   2. It should examine three bits to either side of reference bit in the data train as it appears in a floating window. The floating window allows each reference bit to be examined individually with the pattern to either side which may require precompensation to correct for bit shift.

   3. The patterns, when detected, should be decoded and used to generate control signals to indicate the type of precompensation required, early, on time, or late.

4. In order to get the desired amount of precompensation, a multiple phased WD 2143 clock, or one shots may be used as a delay line. The basic scheme is to write all on time or zero peak shift pulses at a nominal time synchronized to the write clock. These pulses are actually all delayed by 250 nanoseconds. With this scheme early patterns are not delayed in reference to nominal and late patterns are delayed 500 nanoseconds which is actually 250 nanoseconds late as compared to nominal.

This allows for early, on time, and late precompensation with early being 250 nanoseconds prior to on time and late 250 nanoseconds after on time.



— — — — — → Direction of bit shift.
——————→ Direction of Write Precompensation

FIGURE 3-4. PATTERN X 0 1 1 LATE PRECOMPENSATION

When the flux transition pattern of X011 is written on the disk, the first "1's" bit is shifted toward the "0" bit. (This is a data bit cell which may or may not have a flux transition, depending on what was written in the previous cell.) Write precompensation shifts this "1" in the opposite direction the amount of the expected shift.

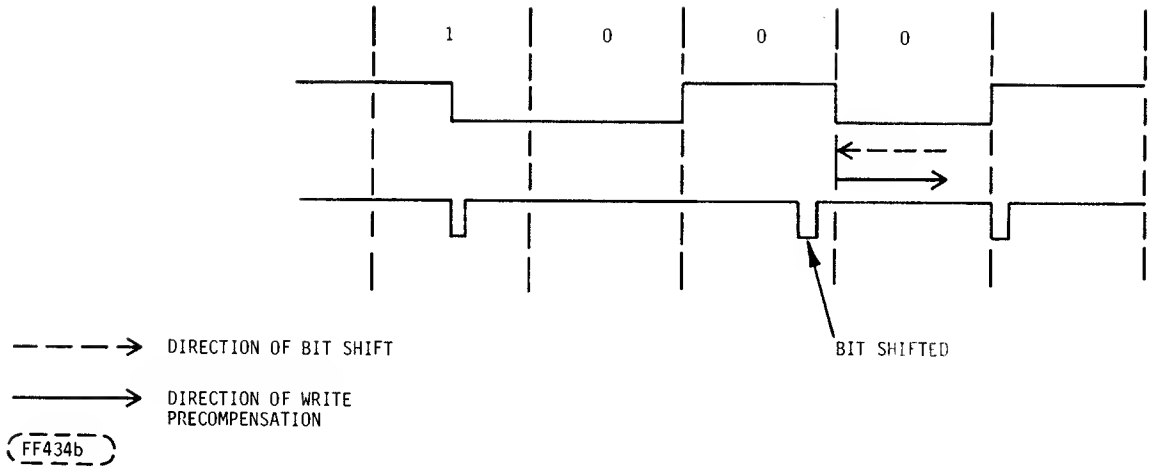


FIGURE 3-5. PATTERN 1000 LATE PRECOMPENSATION

In the case of the 1000 pattern, the second "0" (a clock bit) shifts toward the first "0" (a data bit cell with no flux transition in MFM) and this clock bit is precompensated late, that is, initially it is written closer to the third "0" (also a clock bit).

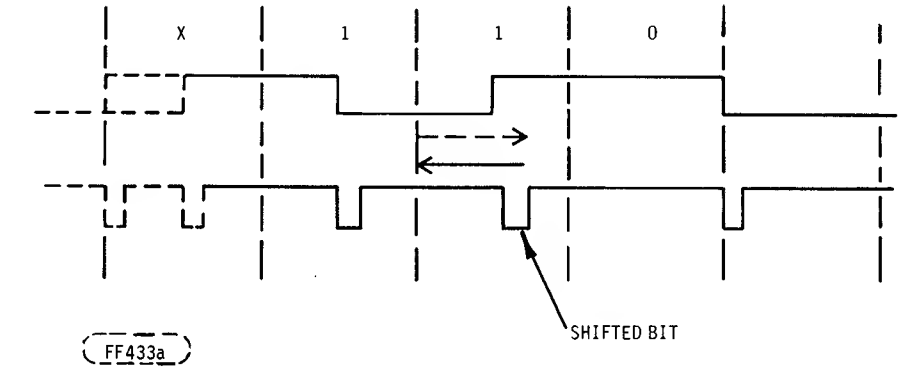


FIGURE 3-6. PATTERN X110 EARLY PRECOMPENSATION

With the pattern X110, the second "1" shifts toward the "0" bit (a bit cell with no flux transition in MFM). This "1" bit is precompensated early, that is, it is written closer to the first "1" data bit. Therefore, in the read back it will appear in the center of the data window.

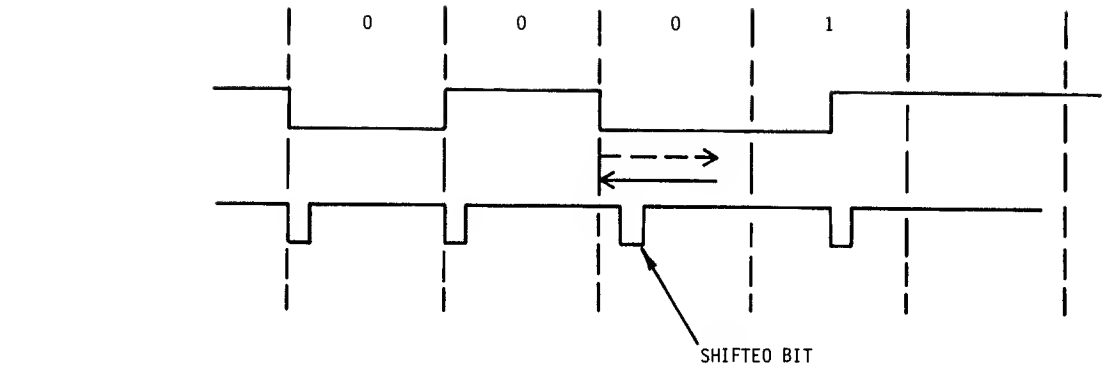


FIGURE 3-7. PATTERN 0001 EARLY PRECOMPENSATION

In the pattern "0001", the third "0" (clock bit from left to right) is shifted toward the "1" data bit. The shifted clock bit is precompensated early toward the second "0" (also a clock bit) to counteract shifting toward the "1".

TECHNICAL INQUIRY

FILE REFERENCE

FROM:

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Name _____

Address _____

City _____

State _____ Zip Code _____

Area Code _____ Phone _____

FOR ADDITIONAL INFORMATION CONTACT:

Flexible Disk
Applications Engineering
Mail Station: OKM 269
Phone: (405) 324-3063

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Oklahoma City, Oklahoma
73157

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